FIGs. 2-4. To form the titanium nitride (TiN) layer 17, a reactive sputtering method can be used, in which the sputtering is effected in an ambient gas of N_2 + argon using a titanium target. The titanium nitride is deposited in a manner that provides complete coverage of the via hole sidewalls and the bottom of the via hole prelined with the titanium aluminide layer 16. A titanium nitride layer having a thickness of approximately 500-1000Å generally is formed. The TiN layer 17 also could be deposited by other known techniques such as CVD. Also, the titanium nitride layer 17 could be replaced by a different type of titanium compound or other sufficiently conductive material that can be deposited as a thin film which provides comparable barrier functionality, such as a Ti-W thin film.

E1

At page 8, first partial paragraph:

E2

A refractory metal plug 14 is then deposited in the titanium aluminide/TiN-lined via hole 200. The refractory metal plug layer, such as tungsten, molybdenum, titanium, tantalum, or the like, can be deposited by CVD to conformally blanket coat the lined via hole and adjoining dielectric flats of the intermediate device structure. For instance, tungsten (W) can be deposited in the lined via hole 200 by conventional CVD methods using a hydrogen and/or silane hydrogen reduction of tungsten hexafluoride (WF_6) in which the premixed reactant gases are directed onto the surface of the intermediate semiconductor structure having the lined via holes to be coated, which is maintained at an elevated temperature of approximately 440-450°C for a process time that is sufficient to fill the lined via hole. When the mixed gases contact the substrate surface at the elevated temperature, the tungsten hexafluoride and the hydrogen (and/or silane) react to produce elemental tungsten (W), which is deposited upon onto the substrate as a film. A via or vertical interconnect structure has been formed at this juncture of the processing. The refractory metals can be used individually, as combinations thereof, or in combination with other low resistance materials to form the plug.

At page 9, first partial paragraph:

E3

FIG. 2 shows an enlarged view of the via of FIG. 1 as fabricated according to a first embodiment of this invention. The via hole 200 is defined by a bottom 200' and sidewalls 200". The bottom 200' of the via hole 200 is the exposed surface of the underlying interconnection layer 12 until the via hole 200 is lined. The dielectric layers 11 and 13 and the ARC layer 18 are the same as described in connection with FIG. 1. Titanium aluminide 16 is directly sputter deposited on the via hole 200. To accomplish this, a titanium aluminide target is used in a sputtering chamber at approximately 2 kW dc target power at 1.5 mtorr pressure. When depositing titanium aluminide directly by sputtering, the titanium aluminide layer is formed at a thickness of approximately 100 to 700Å, preferably about 400Å, to provide the barrier properties desired of it.

At page 9, last partial paragraph, to page 10:

E4

In one preferred implementation, the titanium aluminide layer 37 is formed by annealing at approximately 140 seconds at a 465°C chuck temperature in a chamber. An approximately 50 to 300Å titanium layer can deposited and the annealing is performed for a time sufficient such that the titanium at the bottom of the via hole 300 is substantially if not completely reacted with surface portions of the underlying aluminum conductor line 31 to form the titanium aluminide layer portion 37 at the bottom 300' of the via hole 300. The resulting titanium aluminide layer portion 37 can have a thickness of approximately 100 to 700Å, preferably about 400Å, to provide the barrier properties desired of it. The titanium film deposited to line the sidewalls 300" and out of contact with aluminum of via hole 300 remains elemental titanium after the titanium aluminide formation.

At page 10, second full paragraph:

E5

Experimentation has been performed which demonstrated and confirmed the barrier attributes possessed by the titanium aluminide layers formed according this invention. Specifically, 200Å of Ti was deposited on top of 3.8 kÅ of Al formed on each of two separate Si wafers. A first Ti-coated wafer was heated in an anneal chamber to a temperature and for a time sufficient to form $TiAl_3$ by reaction of substantially all the Ti

film with the contacted aluminum surface. The second Ti-coated wafer was not annealed. No TiN barrier layer was deposited over either test wafer. Then both wafers were subjected to fluorine attack in a CVD reactor chamber by exposure to WF_6 and heat of approximately 440°C. This comparative test represented a worst case scenario by creating an environment comparable to cracking in a TiN barrier layer of where the TiN layer is discontinuous at the via bottom. As to the results of the experimentation, when viewed under high magnification, the first wafer having the $TiAl_3$ surface layer formed on the Al had no significant indications of fluorine attack. By contrast, the bare Ti-coated wafer suffered extensive fluorine attack seen as a dense cluster of island-like spots all across the surface of the Ti film. These results demonstrated that preformed titanium aluminide layers have high resistance to fluorine attack. Therefore, the preformed titanium aluminide layer formed in this invention provides a back-up measure of protection, in addition to the TiN barrier layer, against fluorine attack during fabrication of the vias.

E5

In the Claims:

Please replace the respective claims with the amended claims as follows:

28. (Five Times Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

E6

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the semiconductor substrate;

an antireflective coating over said first metallic layer;